An Impedance Model for the Quasi-Optical Diode Array

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Abstract—**A circuit representation is presented for the quasi-optical impedance of an infinite array of strips or slots periodically loaded with two terminal semiconductor devices (diode array). The circuit elements are obtained by method of moments analysis of the equivalent waveguide discontinuity problem. A set of design curves for the circuit model components at 99 GHz is provided. The curves are applicable at other frequencies by scaling. For the strip array, the results indicate the presence of a substantial capacitance in parallel with the diode. This capacitance can be substantially reduced by incorporation of an appropriately designed "rectangular unit cell." A slot version of the diode array has also been simulated and modeled, and may prove useful in future applications.**

I. Introduction

In recent years, monolithic diode arrays (grids) have been experimentally demonstrated as quasi-optical frequency multipliers and phase shifters [1]–[3]. Such arrays have potential application as components in millimeter-wave systems for beam transmission, reception, and imaging. A standard unit cell layout for a diode array is shown in Fig. 1. The vertical metal strips are often connected with horizontal strips, to provide dc bias. The bias strips, however, are perpendicular to the electric field, and should not appreciably affect the electromagnetic behavior. Under the quasi-optical approximation, the diode grid is modeled as a lumped impedance in a transmission line representation of the system in which it is embedded. The grid impedance Z_g can be obtained by considering the unit cell of the array as a planar discontinuity between two TEM waveguides [4], which represent the media between which the diode grid is located.

II. Theory

In previous diode array designs, a quasi-static inductance [5] was used to model the electromagnetic behavior. The accuracy of this solution is limited by its assumption of a uniform strip current. For a more accurate solution, a modal analysis [6] or a method of moments solution could be employed; the latter having been chosen for the current work.

The strip is assumed to be infinitesimally thin and perfectly conducting. It is assumed sufficiently narrow that the current flows only in the parallel direction and is uniformly distributed along the perpendicular axis. The longitudinal distribution of the current is modeled by piecewise sinusoidal segments.

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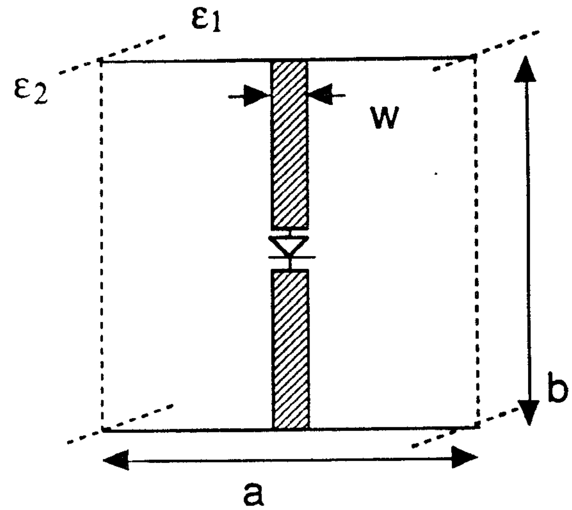

Fig. 1. Illustration of the unit cell of the strip diode array, in which the electric field and current are oriented parallel to the strip.

The subdomain current amplitudes I_l can be obtained from the method of moment equation

$$E_{\text{inc}} = \frac{1}{ab} \sum_{l=1}^{N_E} I_l \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \tilde{G}_{yy} \tilde{\hat{K}}_l \tilde{\hat{K}}_k^*, \qquad (1)$$

for the kth subdomain element, where E_{inc} is the TEM electric field at the dielectric interface in the absence of the strips, N_E is the number of subdomain elements, $\tilde{\hat{K}}$ is the transform of a normalized subdomain current function, and $\tilde{G}_{yy}$ is the Green's function, which can be found by a TE/TM transmission line [7] analysis. By relating the scattered TEM field to the method of moments currents and relating the grid impedance to the scattered TEM field by reflection coefficient considerations, the solution for the grid impedance

$$Z_g = \frac{ab}{\sum_{l=1}^{N_E} I_l} - Z_{00} \qquad (2)$$

is obtained, where Z_{00} is the TEM input impedance seen at the grid. The diode is simulated by addition of a self-impedance term for the segment at which the diode is located which is proportional to the diode impedance.

III. Numerical Results

The circuit of Fig. 2 was tested as a possible model for the grid impedance of Fig. 1. The component values were ob-

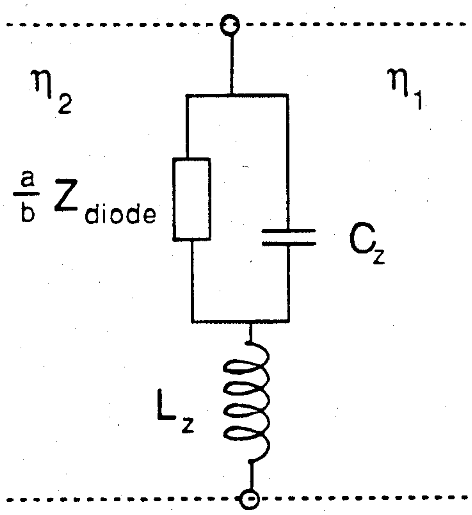

Fig. 2. Schematic representation of the model of the diode grid impedance Z_g for the strip diode array.

tained by performing the analysis on the cases of open and short circuited diode. Comparisons of the numerical solution and the circuit model for numerous geometries tested over the full range of diode impedance gave agreement within 1.1% in all cases.

Previous arrays have employed a square ($a = b$) unit cell, but this is not required. For nonsquare arrays, the model must use a diode impedance scaled by the factor a/b. The numerical solution shows this to be the case, and it is consistent with the observation that the transmission line model implicitly assumes a square unit cell. The scaling of diode impedance with cell shape offers potential performance benefits with respect to power handling capability and ease of device fabrication.

The solution is also applicable to the dual problem involving a diode-loaded array of horizontal (perpendicular to the incident electric field) slots. The model of the slot array consists of an inductance L_y in series with the diode (counterpart element to C_z) and a capacitance C_y across the series combination of diode and inductance (counterpart element to L_z).

Simulations were run for the case of a diode grid at an air-Gallium Arsenide ($\epsilon_r = 12.9$) interface at 99 GHz. The elements L_z and C_y of the strip and slot arrays, respectively, are shown in Fig. 3. The inductance is seen to closely follow the quasistatic result, and the capacitance can be found to closely follow its quasistatic counterpart for a homogeneous medium of effective dielectric constant $(\epsilon_{r1} + \epsilon_{r2})/2$. Fig. 4 illustrates the elements C_z and L_y of the strip and slot arrays, respectively. The graphs illustrate the dramatic reduction of C_z obtainable by a decrease in the unit cell height b. The capacitance is reduced due to two effects. First, it undergoes an "in series" scaling effect based on unit cell shape analogous to that of the diode impedance. Second, it is further reduced by the fact that the individual capacitances which are now "in series" are themselves smaller because they are those of a more closely spaced grid.

The results can be applied at other frequencies by scaling all dimensions, capacitances, and inductances by ω^{-1}.

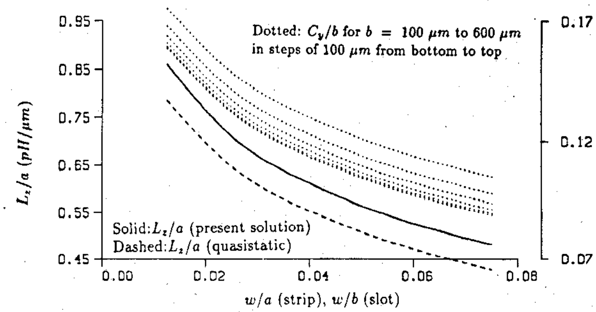

Fig. 3. Results at 99 GHz for the component elements L_z/a and C_y/b for the strip and slot diode array, respectively, at an interface of Gallium Arsenide ($\epsilon_r = 12.9$) and air. $N_E = 80$ for all cases.

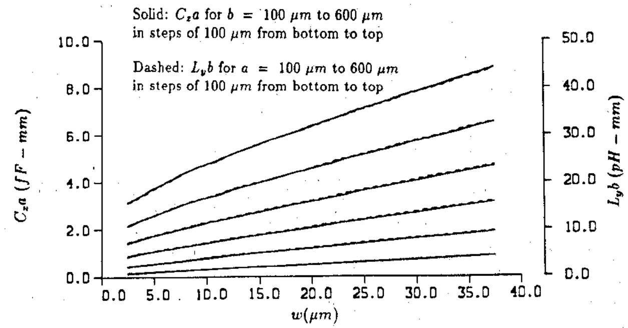

Fig. 4. Component elements $C_z a$ and $L_y b$ versus w (μm) for the strip and slot diode array, respectively, of Fig. 3. The graphs for $C_z a$ and $L_y b$ are virtually indistinguishable from each other.

While C_z is an inherent property of the periodic grid, specific array designs may posses some additional capacitance, which should also be considered, associated with layout-specific features such as anode and cathode fingers.

High frequency circuits employing varactor diodes typically require a small $C_{\min}$ for good performance. An array example is the proposed 360 degree quasi-optical stacked array [1] phase shifter, currently under active development [8], which requires a minimum capacitance of 7 fF. For the array dimensions required for diode grids in the 100 GHz region, the current work indicates that C_z for a square unit cell will be 7–10 fF, precluding the possibility of achieving 360 degrees of phase range. An optimized design with a square unit cell shows 504 degrees of phase range without C_z considered in the simulation. The range is reduced to 258 degrees when C_z is included in the model. However, reduction of the b dimension by a factor of 2.5 increases the simulated phase range to 464 degrees. This feature has therefore been incorporated into the 360 degree phase shifter design.

IV. Conclusion

An improved circuit model has been devised for the quasi-optical impedance of a diode-loaded strip array. The model indicates the presence of a substantial capacitance in parallel with the diode, which should be taken into account in array design. The use of a different diode spacing along each axis ("rectangular unit cell") shows promise as a solution to suppress the undesired capacitance. A slot array counterpart to the strip array has also been analyzed, and may be of interest for future applications.

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